SEE Test Report V1.0
Heavy ion SEE test of SIDECAR ASIC from TELEDYNE/UMC

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I. Introduction

This study was undertaken to determine the single event susceptibility of the SIDECAR ASIC for destructive events induced by exposing it to a heavy ion beam at the TEXAS A&M Cyclotron Single Event Effects Test Facility. This test will be performed in the frame of HST project.

II. Devices Tested

The sample size of the testing is three devices coming from JWST flight lot and provided by Teledyne.

The device technology is CMOS 0.25 µm from UMC. The device is packaged in a custom metal package. The device under test (DUT) lid frame was be removed.

SIDECAR ASIC was previously tested to protons at cryogenic temperature for JWST project. No proton induced SEL was observed. Uncorrectable errors in digital section were only observed at high proton flux when two protons hit two separate bits of the same data word. Few Single Event Transients (SET) were observed in the analog section.

III. Test Facility

Facility: TEXAS A&M Cyclotron Single Event Effects Test Facility, 25 MeV/u beams
Flux: 1.9×10^3 to 4.7×10^5 particles/cm^2/s.
Fluence: All tests were run to 1×10^7 p/cm^2 or until SEL or SEFI events occurred

The ions and corresponding LET values used for these tests are shown in Table 1. Energy and LET values given in the Table are Energy and LET at the target. Penetration range of these ions in Silicon is greater than 200 µm. Main goal of this test was Single Event Latch-up (SEL) characterization. Therefore, most of irradiations were performed with Xe ions and a DUT heated to a temperature of 75°C. Figure 1 shows the SIDECAR ASIC in front of the beam output at TEXAS A&M.

Table 1: Characteristics of ions used for the tests

Ion	Energy at target (MeV)	LET at target and normal incidence (MeVcm^2/mg)
Xe	2830	40.2
Kr	1895	20.4
Ar	939	5.7

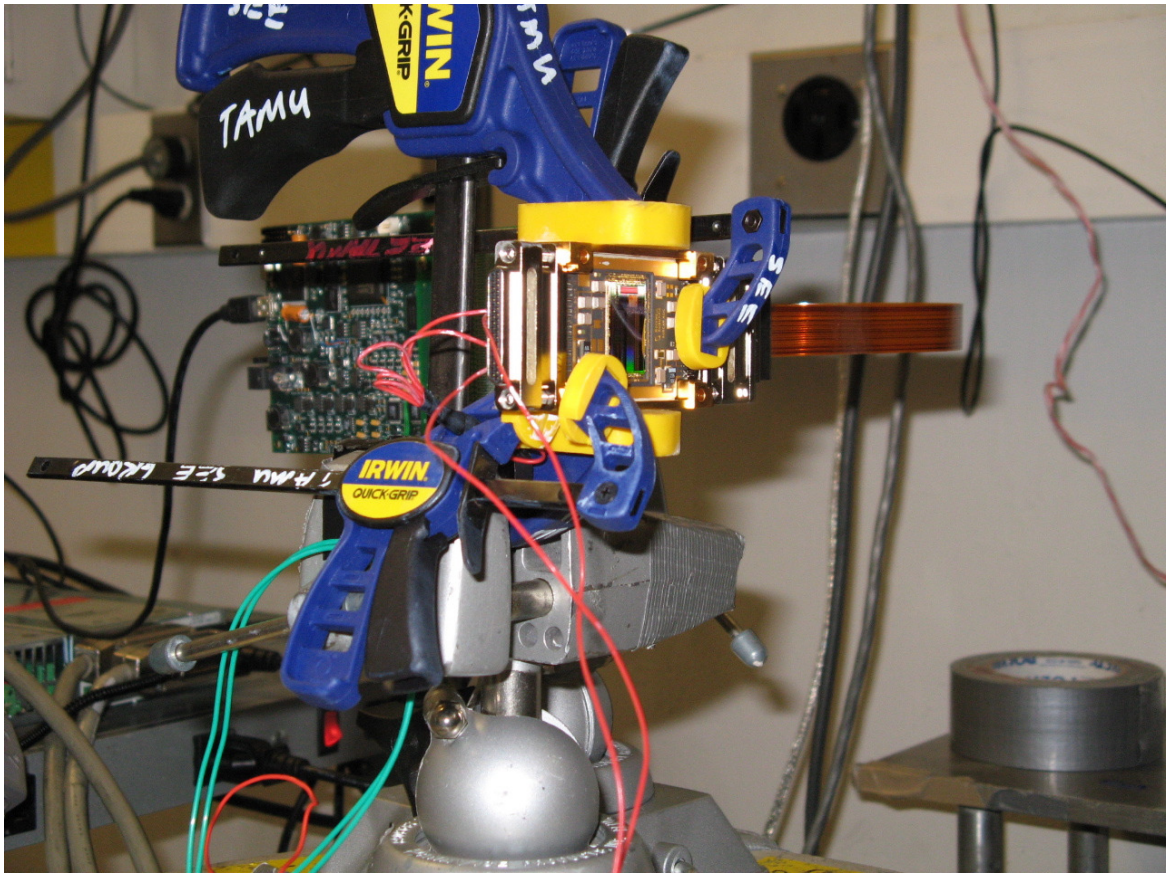

Figure 1: SIDECAR ASIC in front of beam line

IV. Test Conditions and Error Modes

Test Temperature: 75ºC case and room temperature
Bias conditions Vdda = 3.3V
Vdd2V5 = 2V (logic)
Vdd3V3 = 3.3V (clk)
Vddio = .8 or 1.2V
Vref= 3.3V

PARAMETERS OF INTEREST: Power supply currents, DUT functionality, 2Kx2K data array (imaging program), error counts in memory (memory program)

SEE Conditions: SEL, SEDR, SEU, SET, SEFI

V. Test Methods

Test set-up is described shortly in Teledyne test plan reference QP-XXXX draft. Two test programs have been used for these tests. First one is an imaging test. When imaging test is running, a 2Kx2K array is acquired every 10 second. Data stored in the array is made of two 1Kx2K Analog to Digital Conversions by the DUT of its internal references. Changes in the references , preamps/ADCs recorded in the data array are therefore available for post analysis

Second test program is a memory test program. SIDECAR ASIC microcontroller executes NOP (no operation). As a result instruction memories are filled with 0s. We only look at readback telemetry during memory tests. SIDECAR ASIC instruction memory is protected from SEU with a Single Error Correct Double Error Detect (SECDED) Hamming code. Each word of instruction memories are scrubbed every 1.6 ms. Scrubbing telemetry is available in real time during the test for both data and instruction memory. For this test we were only interested in instruction memory telemetry: SEU count (4-bit counter rollover), corrected error count (4-bit counter rollover), double error count, (4-bit counter rollover. Size of instruction memory is 16Kx16 bits. Size of data memory is 8Kx8 bits.

In case a test stops during an irradiation because of a Single Event Functional Interrupt (SEFI), irradiation is stopped and a SEFI event is recorded. DUT functionality is restored (via reset, reload of test programs, or power cycle), and another irradiation is started up to the next event. A SEFI is detected when communication between SIDECAR ASIC and computer controlling the tests and collecting the data is lost.

During image test, power supplies are monitored every 2.5second, and recorded during the test. As soon as one of the power supply current is above latch-up threshold limit for more than 20 seconds, test is stopped, power supplies are cycled and one SEL event is recorded. As soon as one of the power supply currents reached a maximum limit, test is stopped and power supplies are cycled, and one SEL event is recorded. After a SEL another test run is started up to the next event. Table 2 gives the nominal power supply currents, SEL threshold limits, and the maximum limits.

Table 2: Latch-up criteria

	Voltage (V)	Nominal current (mA)	initial SEL criteria (mA)	Updated SEL criteria (mA)	Maximum limit (mA)
Vdda	3.4	10.7	10	15	20
Vref	3.3	0.025	0.03	0.04	0.05
Vdd3.3	3.3	1.34	1.4	1.6	2.8
Vdd2.5	2	2.12	4.2	5	7.5
Vddio	1.3	1.52	1.85	2.2	3.6

VI. Test Results

Test log is shown in Appendix. Table 3 gives a summary of SEL test results. Minimum and maximum confidence limits are 95% confidence limits of measured cross-sections. Only one SEL event was observed during the test. SEL event was observed on Vdd2.5 power supply at the highest tested LET of 80 MeVcm^2/mg and at high temperature. SEL current was about 35 mA. DUT recovered after power cycle.

During one irradiation run, run 3, we also observed one over-current on Vdda. Vdda reached the 10mA threshold that was initially set for SEL. Over-current condition did not disappear after power cycle. After analysis, it appeared that it was a normal thermal increase of power supply currents, and SEL threshold limits were changed. Figure 2 shows the SEL cross-section curve. It should be noted that with only 1 event, test statistics is very low. SEL LET threshold can be anywhere between 56.9 and 80.4 MeVcm^2/mg.

Table 3: SEL test results summary

SN #	Temp (°)	Ion	Angle (degrees)	Eff. LET (MeVcm^2/mg)	Fluence (#/cm^2)	SEL #	SEL Xsection (cm2/dev)	CLmin (cm^2/dev)	CLmax (cm^2/dev)
60	25	Ar	0	5.7	1.92E+07	0	0.00E+00	0.00E+00	1.56E-07
60	25	Ar	45	11.4	2.00E+07	0	0.00E+00	0.00E+00	1.50E-07
60	25	Kr	0	20.4	1.10E+07	0	0.00E+00	0.00E+00	2.73E-07
60	25	Kr	45	28.8	8.43E+06	0	0.00E+00	0.00E+00	3.56E-07
14	75	Xe	0	40.2	1.29E+07	0	0.00E+00	0.00E+00	2.32E-07
60	25	Kr	60	40.8	1.20E+07	0	0.00E+00	0.00E+00	2.51E-07
14	75	Xe	45	56.9	1.03E+07	0	0.00E+00	0.00E+00	2.90E-07
14	75	Xe	60	80.4	1.09E+07	1	9.17E-08	2.32E-09	5.11E-07

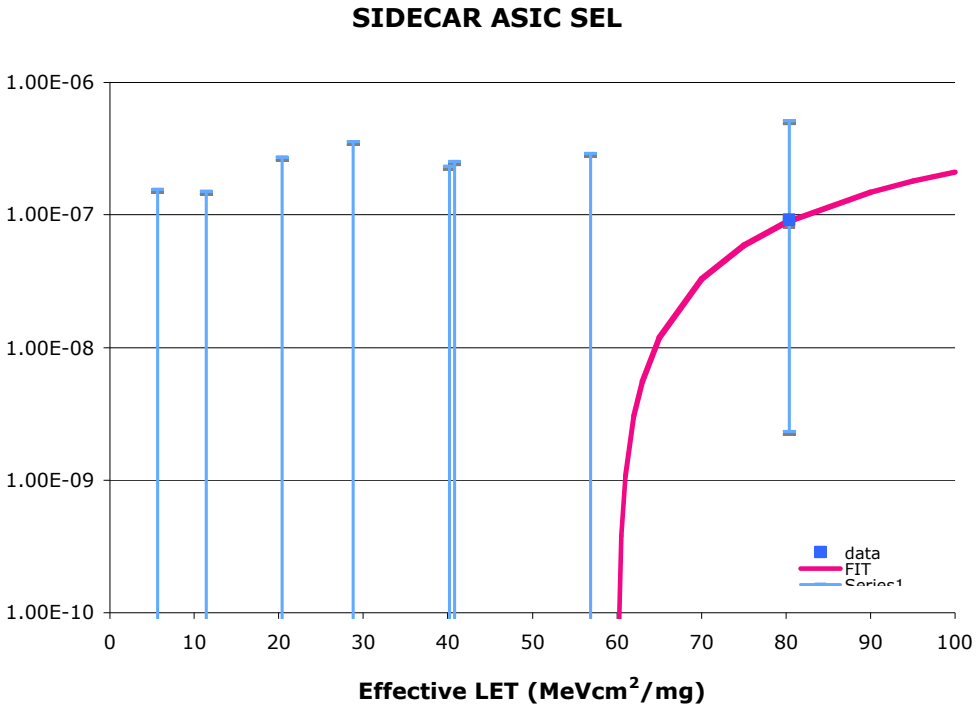

Figure 2: SEL cross-section curve

Summary of SEFI test results is shown in Table 4. Generally a reset is sufficient to recover from a SEFI. But on one occurrence during a memory test (run 29), processor halted and a power cycle was necessary to recover. Figure 3 shows a plot of SEFI cross-sections versus LET. We can see that DUT is little bit less sensitive with the memory program. DUT is sensitive to heavy ion induced SEFI down to a LET of 5.7 MeVcm^2/mg. This indicates a possible sensitivity to proton-induced SEFIs.

We don't know the cause of SEFI. One possible cause of SEFI is the occurrence of uncorrectable errors in an instruction code word. These double errors were unexpected because each of the 22 bits composing an instruction word are far apart (~200 µm). Fluxes were low enough and scrubbing fast enough (1.6ms) to assure that the probability of two single particles hitting the same memory word is very low. Another issue is that digital voltage Vdd2.5 was set at 2V instead of 2.5V. It is known that reducing power supply voltage increases SEU sensitivity.

Memory error counts collected during the test were not accurate because four bits counters were used to count the events. Therefore, after 15 counts, counter goes back to 0.

Degradations were observed on the frames during irradiation. They were generally, but not always, precursor of a SEFI.

Table 4: Summary of SEFI test results

Memory									
DUT #	**Temp (°)**	**Ion**	**Angle (degrees)**	**Eff LET (MeVcm^2/mg)**	**Fluence (#/cm2)**	**SEFI #**	**SEFI Xsection (cm^2/dev)**	**CL min (cm^2/dev)**	**CL max (cm^2/dev)**
60	25	Ar	0	5.7	9.98E+06	0	0.00E+00	0.00E+00	3.01E-07
60	25	Kr	0	20.4	9.98E+06	0	0.00E+00	0.00E+00	3.01E-07
60	25	Kr	45	28.8	8.43E+06	2	2.37E-07	2.87E-08	8.58E-07
14	75	Xe	45	56.9	2.75E+06	2	7.28E-07	8.81E-08	2.63E-06
14	75	Xe	60	80.4	2.00E+06	1	5.00E-07	1.27E-08	2.79E-06
Imaging									
DUT #	**Temp (°)**	**Ion**	**Angle (degrees)**	**Eff LET (MeVcm2/mg)**	**Fluence (#/cm2)**	**SEFI #**	**SEFI Xsection (cm^2/dev)**	**CL min (cm^2/dev)**	**CL max (cm^2/dev)**
60	25	Ar	0	5.7	9.21E+06	1	1.09E-07	2.75E-09	6.05E-07
60	25	Ar	60	11.4	1.00E+07	0	0.00E+00	0.00E+00	3.00E-07
60	25	Kr	0	20.4	9.90E+05	1	1.01E-06	2.56E-08	5.63E-06
14	75	Xe	0	40.2	1.29E+07	13	1.01E-06	5.36E-07	1.72E-06
60	25	Kr	60	40.8	1.77E+06	1	5.65E-07	1.43E-08	3.15E-06
14	75	Xe	60	80.4	4.22E+06	9	2.13E-06	9.76E-07	4.05E-06

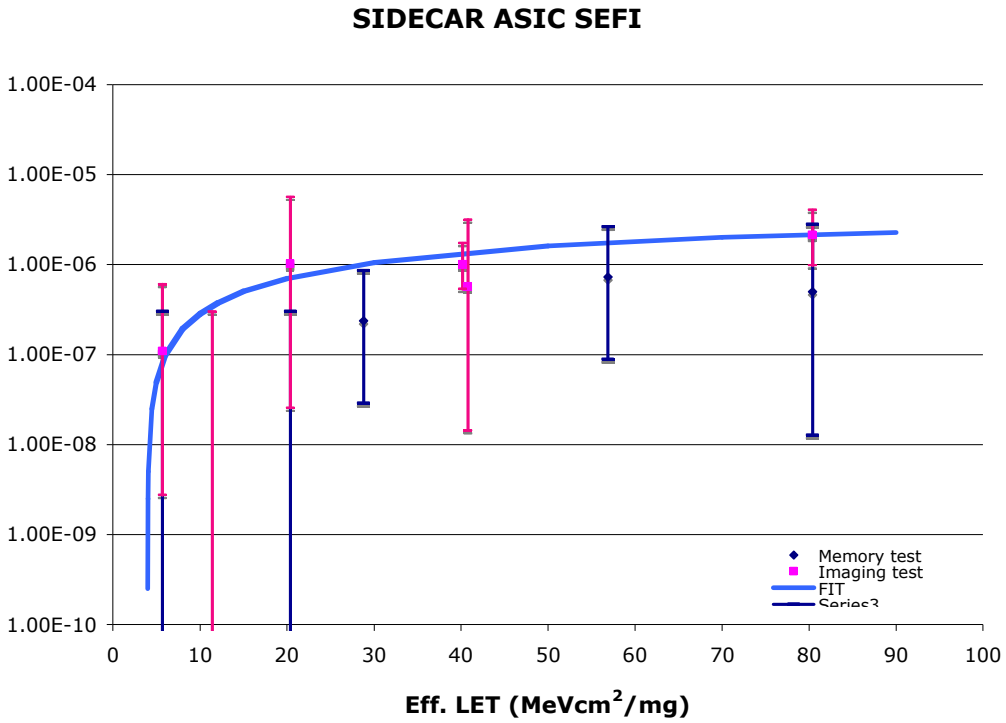

Figure 3: SEFI cross-section curve

VII. Laser Testing

Laser testing was performed at Naval Research Laboratory (NRL), Washington, DC pulsed laser facility to get a better understanding of SEFI events observed during heavy ion tests. NRL Laser has a 590 nm wavelength resulting in a skin depth of about 2 μm. Laser spot size is about 1 μm. Pulse rate was set at 1KHz. Laser energy was set at ~74pJ. This is a high energy that corresponds to high equivalent LET (>200MeVcm^2/mg). Vdd2.5 was set at 2.5V. Instruction memory array was irradiated, SEUs were observed, but no double errors were observed. A quick scan of logic and I/O areas did not cause any error. Vdd2.5 was reduced down to 2V as it was set during the heavy ion tests. Again we did not see any double errors in memory and a quick scan of logic area did not cause any error. Vdd2.5 was set again at 2.5V for a quick SEL scan of whole die area. No SEL was detected.

Lens was changed to increase the laser spot size to about 5 μm. Again no double error s were observed when instruction memory was hit with the laser. When running the imaging code, we found a soft spot in logic area that caused an interruption of the frame acquisition (SEFI). After such a SEFI, several double errors were observed in instruction memory. SEFI was reproduced several times when laser hit the sensitive area. In most cases SEFI caused double errors in instruction memory, but not always.

We lowered laser intensity and hit the soft spot again, no error was observed. Intensity was increased back to its initial level and SEFI occurred again. We noticed that SEFI did not occur instantly when we hit the sensitive area with the laser. This led us to think at Single Event transients (SET) that need a clock edge to be captured. Laser pulse frequency was increased to 10 KHz. This did not change anything.

Then, we heated the DUT to 75°C case and a SEL scan was performed on the whole die. No SEL was found.

Then, we changed back to the lens that gives the 1 μm laser spot. The sensitive area was hit and SEFI were created.

Then a specific flip-flop that could be tested in real time was hit. The flip-flop was upset when hit with laser causing 1 to 0 and 0 to 1 transitions.

VIII. Conclusions and Recommendations

SIDECAR ASIC has a low sensitivity to SEL with a LET threshold greater than 59 MeVcm^2/mg. With a rate of 1.9E-16 SEL/day on HST orbit, the probability to have a SEL during the 5-year mission is quasi negligible. SIDECAR ASIC SEL sensitive area was not found during irradiation with the laser. This may be an indication that the event observed was not an actual SEL, but a bus contention in the device. It should be noted that the SEL laser scan was coarse (manual scan). It is therefore possible that we missed the SEL sensitive area.

SIDECAR ASIC has a moderate sensitivity to SEFI. With a rate of 4E-7 SEFI/day on HST orbit, the probability to have a SEFI during the 5-year mission is about 1E-4.. Proton-induced upset may contribute to the SEFI rate. For example, assuming a SEFI proton cross-section of 10^{-13} cm2/dev, the SEFI rate will be increased by a factor 5. We would need more data to confirm that. However, given that the SIDECAR ASIC can be reset or power-cycled should a SEFI occur, these SEFI rates will have no significant impact on the mission.

Laser testing provided further insight on the cause of SEFI. We have seen that double errors in instruction memory were not the cause of SEFI, but, to the contrary, were the consequence of SEFIs. SIDECAR ASIC sensitive area was found in logic area. This was not expected as logic area registers are SEU hardened. Only a simultaneous hit of 2 sensitive nodes that are 10 µm apart may cause an upset of these flip-flops. Laser test has clearly shown that even the small laser spot can generate charges that could diffuse to these 2 sensitive nodes and then upset the register. Laser test has also shown that changing logic area supply voltage Vdd2.5 from 2 to 2.5V does not make much difference.

Test log

Run	Part	DUT #	Test	Temp	ION-energy	LET	Angle	Eff. LET	Flux	Fluence	SEFI	SEL	sig_sefi	sig_sel	Comment
															saw errors in video output then part stopped
1	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	3.18E+04	1.24E+06	1	0	8.06E-07	0.00E+00	functioning; no current anomaly
2	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	5.64E+03	2.73E+05	1	0	3.66E-06	0.00E+00	same
															same; had overcurrent--persisted after refreshes, 10mA
3	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	4.60E+03	6.16E+05	1	0	1.62E-06	0.00E+00	on 3.3Vdda, maybe thermal according to Markus
4	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	5.79E+03	7.18E+05	1	0	1.39E-06	0.00E+00	
5	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	3.17E+04	6.09E+05	1	0	1.64E-06	0.00E+00	
6	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	2.30E+04	5.72E+05	1	0	1.75E-06	0.00E+00	memory test?
7	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	1.93E+04	5.53E+05	1	0	1.81E-06	0.00E+00	ASIC not responding; recovered on reset
8	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	2.29E+04	6.53E+05	1	0	1.53E-06	0.00E+00	FIFO, 11 doubles; reset recovers function
9	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	2.34E+04	9.07E+05	1	0	1.10E-06	0.00E+00	double errors in instruction memory
10	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	2.13E+04	1.63E+06	1	0	6.13E-07	0.00E+00	
11	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	1.87E+04	1.20E+06	1	0	8.33E-07	0.00E+00	error count is modulo 16, count on 4bits
12	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	1.90E+03	1.23E+06	1	0	8.13E-07	0.00E+00	
13	SIDECAR	14	Imaging	75	Xe-2830	40.2	0	40.2	1.95E+04	2.71E+06	1	0	3.69E-07	0.00E+00	
14	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.86E+04	1.97E+05	1	0	5.08E-06	0.00E+00	
15	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.69E+04	2.87E+05	1	0	3.48E-06	0.00E+00	
16	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.95E+04	4.49E+05	1	0	2.23E-06	0.00E+00	
17	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.64E+04	2.72E+05	1	0	3.68E-06	0.00E+00	
18	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.59E+04	5.81E+05	1	0	1.72E-06	0.00E+00	
19	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.71E+04	1.18E+06	?	1	#VALUE!	8.47E-07	SEL on VDD2.5--35.3 mA; recovered after power cycle
20	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.44E+04	1.20E+05	1	0	8.33E-06	0.00E+00	
21	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.64E+04	5.11E+05	1	0	1.96E-06	0.00E+00	
22	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.60E+04	2.36E+05	1	0	4.24E-06	0.00E+00	
23	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.58E+04	1.57E+06	1	0	6.37E-07	0.00E+00	stuck bit? 1 double error remains after resetting, power cycle, OK
24	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.58E+04	1.57E+06	0?	0	#VALUE!	0.00E+00	
25	SIDECAR	14	Imaging	75	Xe-2830	40.2	60	80.4	1.63E+04	3.21E+05	0?	0	#VALUE!	0.00E+00	
26	SIDECAR	14	Mem	75	Xe-2830	40.2	60	80.4	1.43E+04	1.61E+06	0?	0	#VALUE!	0.00E+00	Memory test
27	SIDECAR	14	Mem	75	Xe-2830	40.2	60	80.4	1.50E+04	2.00E+06	1	0	5.00E-07	0.00E+00	Memory test
28	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	7.40E+03	2.75E+04	1	0	3.64E-05	0.00E+00	memory test--processor halted
29	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	8.00E+03	2.72E+06	1	0	3.68E-07	0.00E+00	halted @~2.1E6 had to cycle power
30	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	3.13E+04	2.90E+06		0		0.00E+00	accumulating statistics to look for SEL despite SEFI state
31	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	3.27E+04	2.20E+06		0		0.00E+00	accumulating statistics to look for SEL despite SEFI state
32	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	3.25E+04	1.27E+06		0		0.00E+00	accumulating statistics to look for SEL despite SEFI state
33	SIDECAR	14	Mem	75	Xe-2830	40.2	45	56.9	3.00E+04	1.23E+06		0		0.00E+00	accumulating statistics to look for SEL despite SEFI state
34	SIDECAR	60	Mem	room	Kr-1895	20.4	0	20.4	4.97E+04	9.98E+06	0	0	0.00E+00	0.00E+00	never halted
35	SIDECAR	60	Imaging	room	Kr-1895	20.4	0	20.4	4.70E+05	9.90E+05	1	0	1.01E-06	0.00E+00	old algorithm still crashes
36	SIDECAR	60	maging'	room	Kr-1895	20.4	60	40.8	2.70E+04	1.02E+07	0?	0	#VALUE!	0.00E+00	very few doubles??
37	SIDECAR	60	Imaging	room	Kr-1895	20.4	60	40.8	2.68E+04	1.77E+06	1	0	5.65E-07	0.00E+00	old algorithm still crashes, but ran much longer
38	SIDECAR	60	Mem	room	Kr-1895	20.4	45	28.8	2.57E+04	2.50E+06	1	0	4.00E-07	0.00E+00	new algorithm (memory test) did crash
39	SIDECAR	60	Imaging	room	Kr-1895	20.4	45	28.8	2.40E+04	5.93E+06	1	0	1.69E-07	0.00E+00	
40	SIDECAR	60	Mem	room	Ar-939	5.7	0	5.7	4.79E+04	9.98E+06	0	0	0.00E+00	0.00E+00	
41	SIDECAR	60	Imaging	room	Ar-939	5.7	0	5.7	4.38E+04	9.21E+06	1	0	1.09E-07	0.00E+00	old algorithm crashed
42	SIDECAR	60	Mem	room	Ar-939	5.7	60	11.4	4.44E+04	9.99E+06	0	0	0.00E+00	0.00E+00	
44	SIDECAR	60	Imaging	room	Ar-939	5.7	60	11.4	1.51E+05	1.00E+07	0	0	0.00E+00	0.00E+00	